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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,970	07/19/2005	Hiroshi Miyagi	TIC-0079	5443
23377	10/20/2006		EXAM	INER
	K WASHBURN LLP	CHEN, JUNPENG		
ONE LIBERTY PLACE, 46TH FLOOR 1650 MARKET STREET PHILADELPHIA, PA 19103			ART UNIT	PAPER NUMBER
			2618	
			DATE MAILED: 10/20/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Applic	cation No.	Applicant(s)		
Office Action Summary		. 10/51	9,970	MIYAGI, HIROSHI		
		Exam	iner	Art Unit	_	
			ng Chen	2618		
 Period for	The MAILING DATE of this commun Reply	nication appears on	the cover sheet with the	correspondence address		
	RTENED STATUTORY PERIOD F	OR REDIVIS SE	T TO EXPIRE 3 MONTH	(S) OR THIRTY (30) DAYS		
WHICH - Extension - after SI - If NO policy - Failure - Any rep	EVER IS LONGER, FROM THE Nons of time may be available under the provisions (6) MONTHS from the mailing date of this comported for reply is specified above, the maximum storeply within the set or extended period for reply received by the Office later than three months patent term adjustment. See 37 CFR 1.704(b).	MAILING DATE OF s of 37 CFR 1.136(a). In n nunication. latutory period will apply a p will, by statute, cause the	THIS COMMUNICATION  o event, however, may a reply be the following will expire SIX (6) MONTHS from the properties of the	DN. timely filed m the mailing date of this communication. IED (35 U.S.C.§ 133).		
Status						
1) 🛛 F	esponsive to communication(s) file	ed on 19 July 2005	5.			
, —	•	2b)⊠ This action				
3)□ S	ince this application is in condition	for allowance exc	ept for formal matters, p	rosecution as to the merits is		
С	losed in accordance with the pract	ice under <i>Ex parte</i>	Quayle, 1935 C.D. 11,	453 O.G. 213.		
Dispositio	n of Claims					
4) 🛛 C	laim(s) <u>1-6</u> is/are pending in the a	pplication.				
4:	a) Of the above claim(s) is/a	are withdrawn from	consideration.			
5) 🗌 C	laim(s) is/are allowed.					
6)⊠ C	laim(s) <u>1-6</u> is/are rejected.					
•	laim(s) is/are objected to.					
8) 🗌 C	claim(s) are subject to restri	ction and/or election	on requirement.			
Applicatio	n Papers					
9)∐ TI	ne specification is objected to by the	ne Examiner.				
	ne drawing(s) filed on <u>30 Decemb</u> e					
	pplicant may not request that any obje					
	eplacement drawing sheet(s) includin					
11)□ T	ne oath or declaration is objected t	o by the Examiner	. Note the attached Office	ce Action or form PTO-152.		
Priority un	der 35 U.S.C. § 119					
12)⊠ A	cknowledgment is made of a claim	for foreign priority	under 35 U.S.C. § 119(	a)-(d) or (f).		
a)⊠						
	. Certified copies of the priority			are a Ala		
	<ul> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage</li> </ul>					
3				ved in this National Stage		
application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.						
36	e life attached detailed Office acti	on for a list of the t	crimed dopies not reder	<b>V33</b> .		
Attachment(	s)					
1) Notice of References Cited (PTO-892)  4) Interview Summary (PTO-413) Paper No(s)/Mail Date						
	of Draftsperson's Patent Drawing Review ( ation Disclosure Statement(s) (PTO/SB/08)			Date  I Patent Application		
	No(s)/Mail Date <u>10/06/2005</u> .		6) Other:			
S. Patent and Trademark Office						

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#### **DETAILED ACTION**

## **Priority**

Receipt is acknowledged of papers submitted <u>under 35 U.S.C. 371 and 35</u>
 <u>U.S.C. 119(a)-(d)</u>, which papers have been placed of record in the file.

#### Information Disclosure Statement

2. The information disclosure statement submitted on <u>October 06, 2005</u> has been considered by the Examiner and made of record in the application file.

## Objection - Drawing

3. The drawings are objected to because block 25 in figure 5 lacks descriptive label. For example, it should be additionally labeled as: "Smoothing Circuit". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application

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must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

## Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Consider **claim 4**, applicant recites "a *charge circuit for charging* the capacitor at intervals in case where the *input voltage is relatively higher than the terminal voltage*". However, claim 4 further claims "a *discharge circuit for discharging* a discharge current at intervals from the capacitor in a case where the terminal voltage is relatively lower than the input voltage". While "input voltage is relatively higher than the terminal voltage" is the same as "the terminal voltage is relatively lower than the input voltage", two opposite operations, namely, charging and discharging, are performed. As a result of above two contradictive limitations, they render claim 4 indefinite.

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## Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 6. Claims 1, 3 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Etsuya Shibata (JP10-270961-A) (See attached English Translation by Thomson).

Consider claim 1, Etsuya Shibata discloses an AGC circuit (read as automatic gain control circuitry, Abstract) comprising a detection circuit that detects a high frequency reception signal and outputs a detection signal including a pulsating component (read as video detector circuit 3 detects video signal, which inputs into detector circuit 4, the output of detector circuit 4, which is detection voltage, includes pulsating-current component, Figure 1, paragraphs [0014]-[0016]), and controlling a gain of an amplification circuit amplifying the high frequency reception signal according to a detection output of the detection circuit (read as output of smoothing circuit 8 inputs into the variable gain circuit 1 as a gain-control voltage, Figure 1, paragraph [0016]), wherein: a high frequency property of an amplifier that is connected immediately after the detection circuit is deteriorated; or a unit for deteriorating the high frequency property is connected to the amplifier (read as smoothing circuit 8 is connected amplifier circuit 5, Figure 1, paragraph [0015]).

Consider **claim 3**, as applied to claim 1 above, Etsuya Shibata discloses that wherein the unit for deteriorating the high frequency property is a capacitor with large

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capacity that is connected between an output terminal of the amplifier and ground (read as condenser 10 is connected between output of amplifier circuit 5 and ground and its time constant is set up more greatly than the time constant of the detector circuit 4, Figure 1, paragraph [0016]).

Consider **claim 6**, as applied to claim 1 above, Etsuya Shibata discloses that wherein deterioration of the high frequency property is deteriorating by an amount equal to or greater than 3dB in a frequency of the pulsating component (read as Etsuya Shibata discloses the claimed invention as in claim 1, thus, the automatic gain control circuitry by Etsuya Shibata would inherently include what is claimed as in current claim 6. Specifically, the deterioration unit would deteriorating by an amount equal to or greater than 3dB in a frequency of the pulsating component, Figure 1, paragraphs [0014]-[0016]).

## Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
  - Determining the scope and contents of the prior art.

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2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Etsuya

Shibata (JP10-270961-A) in view of Iwahashi (U.S. Patent 5,517,449).

Consider **claim 2**, as applied to claim 1 above, Etsuya Shibata discloses the claimed invention above but fails to specifically discloses that the amplifier circuit 5 whose high frequency property is deteriorated is configured in such a way that a channel length and a channel width is each MOSFET that configures the amplifier are set large up to a degree that the high frequency property of the amplifier deteriorates.

However, in related art, Iwahashi discloses a sense amplifier circuit comprises MOSFETs that are channel width and channel length variable to control the current flowing the cell transistor to enhance data readout speed and making the breakdown voltage becomes high and the programming characteristics will be deteriorated, Figure 19, line 54 of column 18 to line 42 of column 19).

Therefore, it would have been obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Iwahashi into the teachings of Etsuya Shibata for the purpose enhancing data readout speed.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Etsuya Shibata (JP10-270961-A) in view of Hitoshi Kimura (JP57192120A).

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Consider **claim 4**, as applied to claim 1 above, Etsuya Shibata discloses that wherein the unit deteriorating the high frequency property is a smoothing circuit comprising: a capacitor, a charge circuit for charging the capacitor at intervals in a case where the input voltage is relatively higher than the terminal voltage; and a discharge circuit for discharging a discharge current at intervals from the capacitor in a case where the terminal voltage is relatively lower than the input voltage; and the smoothing circuit is connected to an output terminal of the amplifier (read as when the detection voltage fro the detector circuit 4 becomes bigger rapidly, the output voltage of the operational amplifier circuit 5 also becomes bigger rapidly, it charges condenser 10, when the first diode 11 conducts. Moreover, on the contrary, when the detection voltage from the detector circuit 4 becomes smaller rapidly, the output voltage of the operational amplifier circuit 5 also becomes smaller rapidly, the output voltage of the operational amplifier circuit 5 also becomes smaller rapidly, when the 2<sup>nd</sup> diode 12 conducts, the voltage

However, Etsuya Shibata fails to disclose the smoothing circuits comprises a voltage comparison circuit for comparing a terminal voltage with an input voltage of the capacitor.

charged by condenser 10 discharges; and smoothing circuit 8 is connected to output of

amplifier circuit 5, paragraphs [0016] and [0018]).

Nonetheless, in related art, Hitoshi Kimura discloses a comparator 18 to compare output Ee2 and output Ee to control current value to control circuit 14 to obtain accurate output, abstract.

Therefore, it would have been obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Hitoshi Kimura into the

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teachings of Etsuya Shibata for the purpose of allowing the charging circuit and the discharging circuit to make accurate operations according to the result of the comparison.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Etsuya Shibata (JP10-270961-A) in view of Iwahashi (U.S. Patent 5,517,449), and in further view of Nakao Hiroomi (JP2001358319).

Consider **claim 5**, as applied to claim 1 above, Etsuya Shibata disclosed the claimed invention but fails to specifically discloses wherein the amplifier whose high frequency property is deteriorated is configured to increase a wiring capacity up to a degree that the high frequency property of the amplifier deteriorates by arranging respective MOSFETs that configure the amplifier in such a way that wirings among the MOSFETS are crossed with each other.

However, in related art, Iwahashi discloses a sense amplifier circuit comprises MOSFETs that are channel width and channel length variable to control the current flowing the cell transistor to enhance data readout speed and making the breakdown voltage becomes high and the programming characteristics will be deteriorated, Figure 19, line 54 of column 18 to line 42 of column 19).

Therefore, it would have been obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Iwahashi into the teachings of Etsuya Shibata to use the MOSFETs taught by Iwahashi to configure the amplifier for the purpose of enhancing data readout speed.

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However, Etsuya Shibata, as modified by Iwahashi, still fails to discloses wherein the amplifier whose high frequency property is deteriorated is configured to increase a wiring capacity up to a degree that the high frequency property of the amplifier deteriorates by arranging respective MOSFETs in such a way that wirings among the MOSFETS are crossed with each other.

Nonetheless, Nakao Hiroomi discloses the technique of mutually cross-connect transistors by gate wiring portions, abstract.

Therefore, it would have been obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Nakao Hiroomi into the teachings of Etsuya Shibata, which modified by Iwahashi, for the purpose of simplifying the wiring.

#### Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Feilkas; Klaus- Jurgen et al.	US 6816024 B2	Oscillator circuit with switchable compensated amplifiers
Feilkas; Klaus- Jurgen et al.	US 20040100339 A1	Compensated oscillator circuit
Kajigaya; Kazuhiko et al.	US 6160744 A	Semiconductor memory device and defect remedying method thereof

10. Any response to this Office Action should be faxed to (571) 273-8300 or mailed

to:

Commissioner for Patents

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P.O. Box 1450 Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window Randolph Building 401 Dulany Street Alexandria, VA 22314

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junpeng Chen whose telephone number is (571) 270-1112. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Junpeng Chen J.C./jc

October 11, 2006

EDAN ORGAD
PATENT EXAMINER/TELECOMIVAL

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